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(56) Documents Cited
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US 5587332 A

(58) Field of Search
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INT CL[7] H01L 21/8239 21/8246 21/8247 27/112 27/115 29/788

(54) Abstract Title
Triple polysilicon embedded NVRAM cell

(57) An integrated circuit comprises a non-volatile random access memory (NVRAM) array with gates formed in three polysilicon conductive layers 134, 144, 158. The first conductive layer 134 forms the floating gate of an EEPROM cell 122, and the second layer 144 forms wordlines 180, 182 and gates of high voltage (access) FETs 118, 120. Gates of logic FETs 114, 116 are formed from the third conductive layer 158.

The third conductive layer may be used as a mask for the wordlines and high voltage gates.

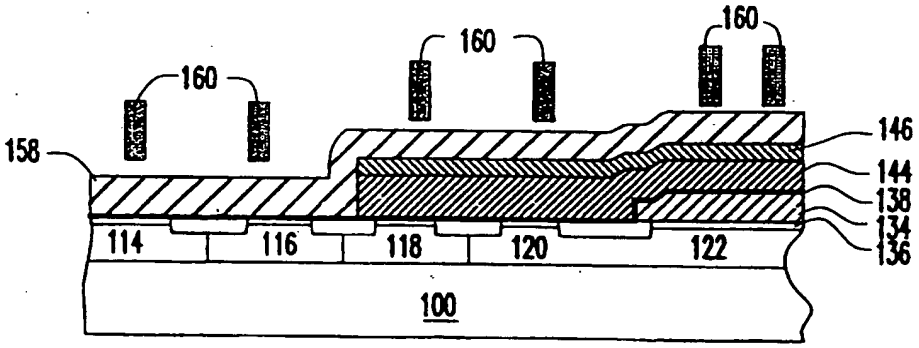

FIG.5B

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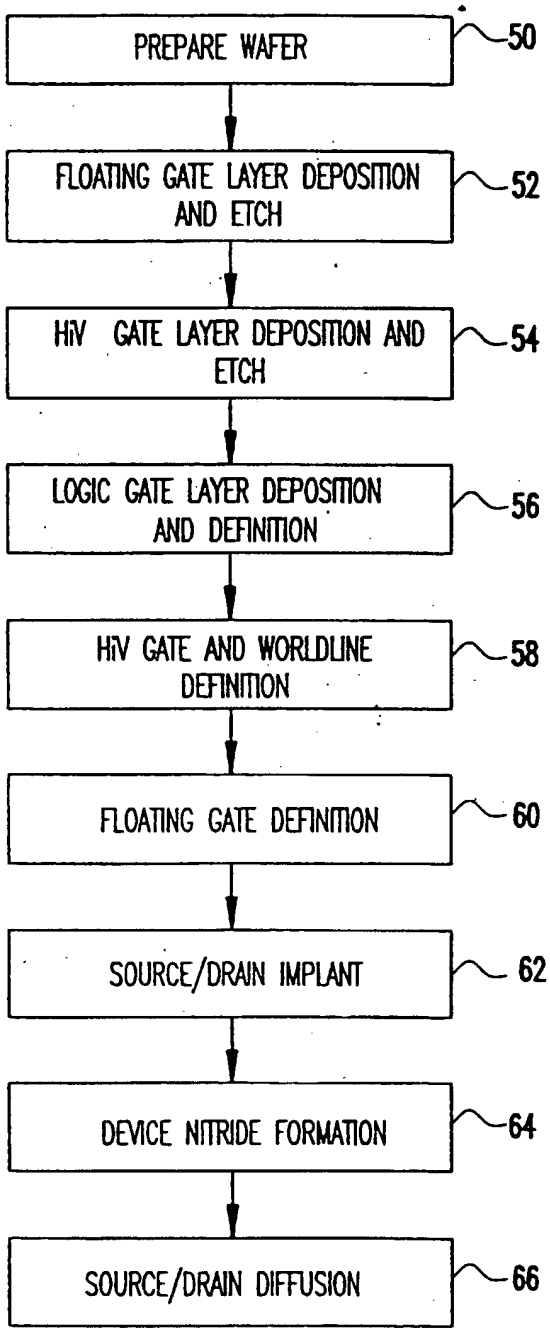
PREPARE WAFER
50
FLOATING GATE LAYER DEPOSITION AND ETCH
52
HiV GATE LAYER DEPOSITION AND ETCH
54
LOGIC GATE LAYER DEPOSITION AND DEFINITION
56
HiV GATE AND WORLDLINE DEFINITION
58
FLOATING GATE DEFINITION
60
SOURCE/DRAIN IMPLANT
62
DEVICE NITRIDE FORMATION
64
SOURCE/DRAIN DIFFUSION
66

FIG.1

PFET 114 NFET 116 HiV PFET 118 HiV NFET 120 EEPROM CELL 122

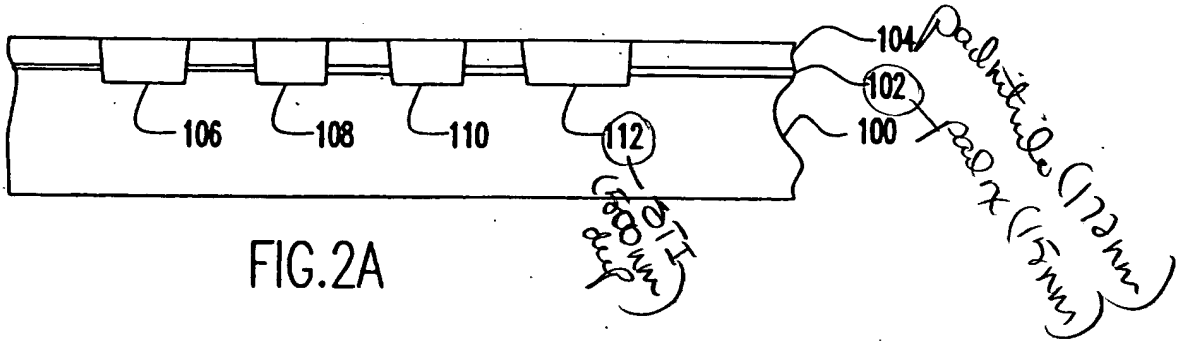

FIG.2A

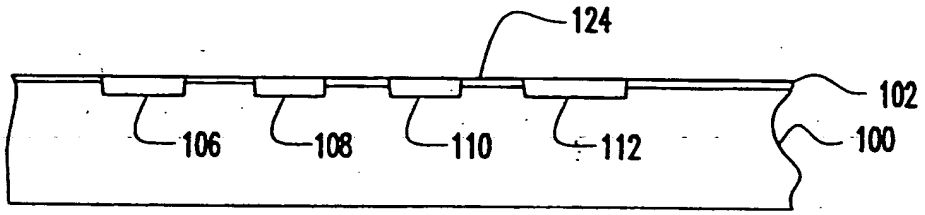

FIG.2B

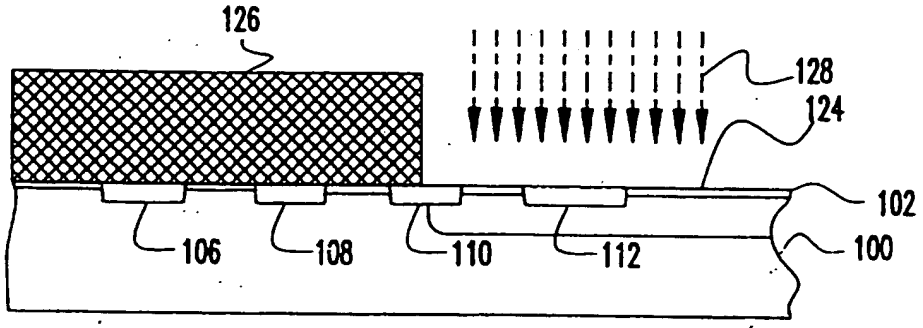

FIG.2C

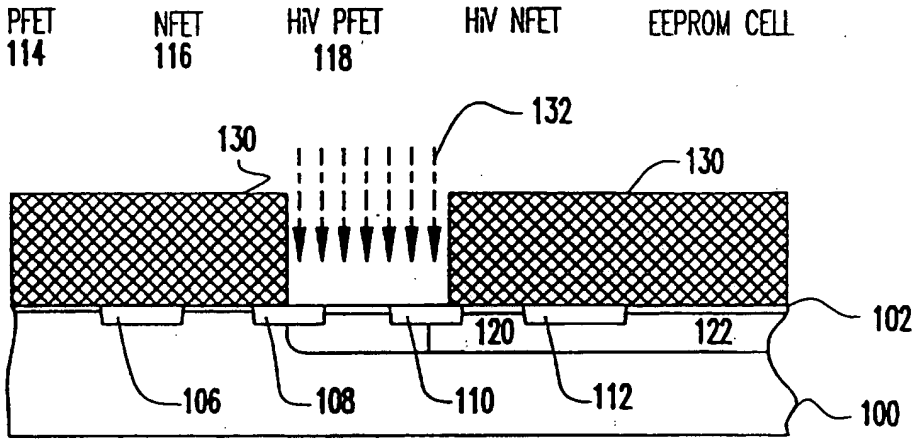

FIG.2D

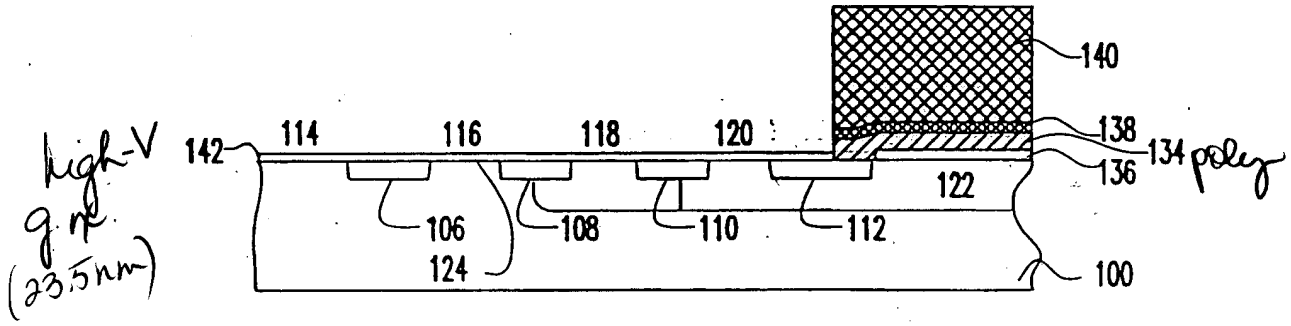

FIG.3

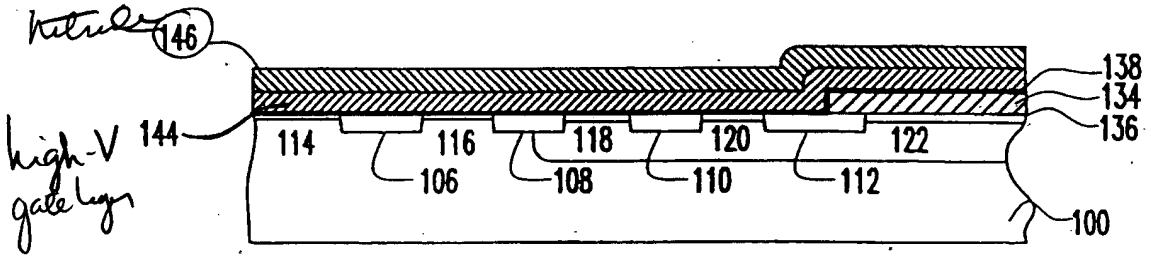

FIG.4A

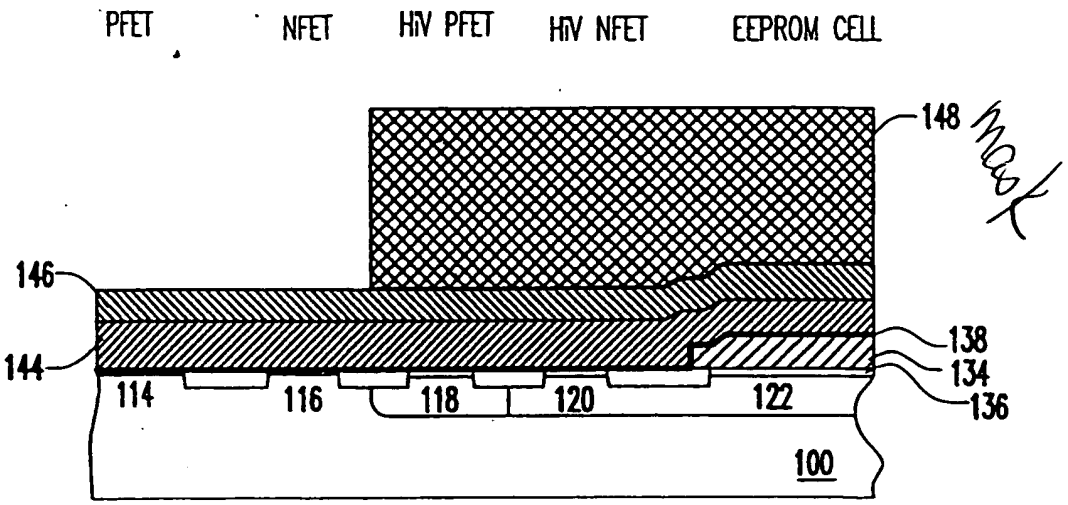

FIG.4B

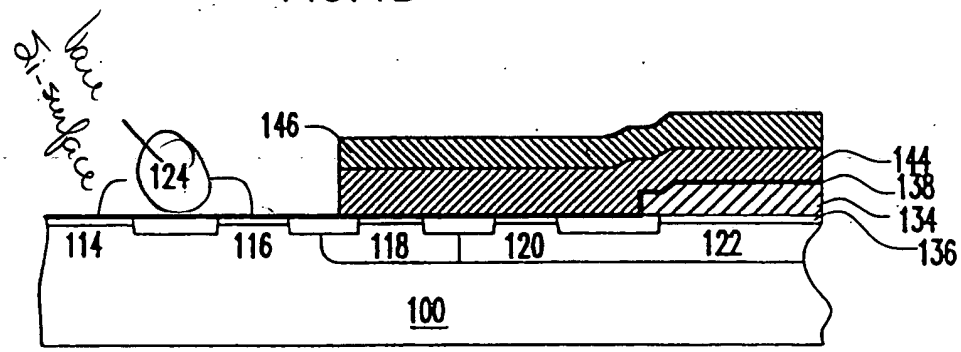

FIG.4C

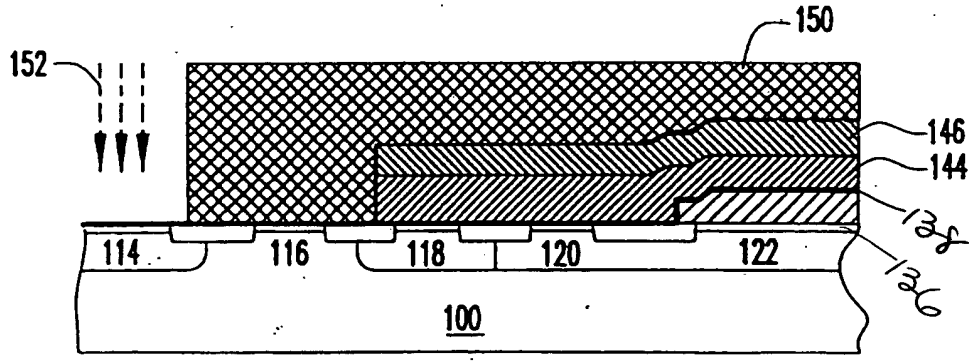

FIG.4D

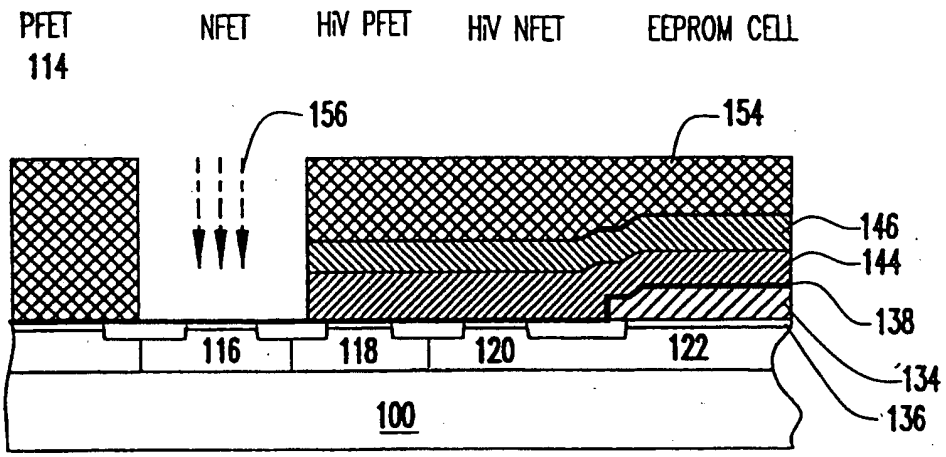

FIG.4E

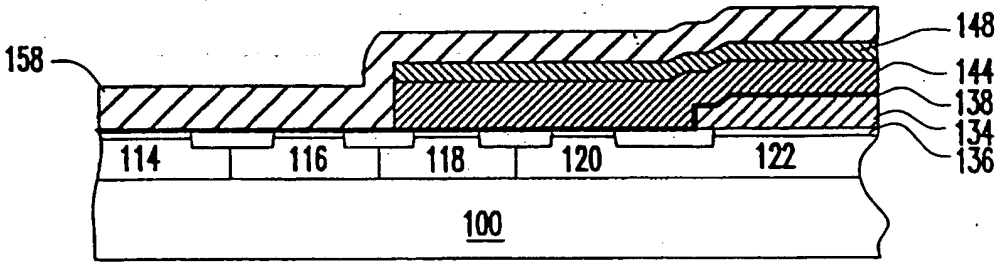

FIG.5A

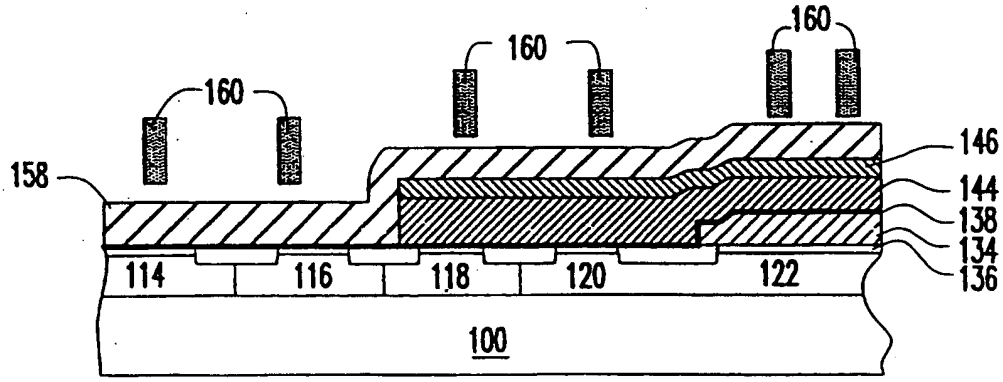

FIG.5B

PFET NFET HiV PFET HiV NFET EEPROM CELL

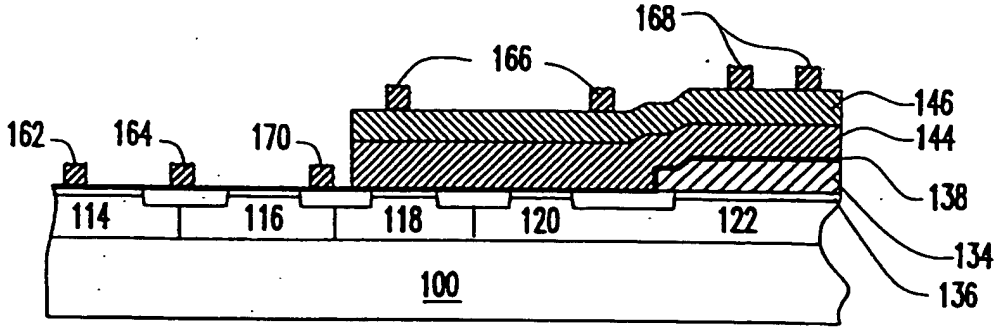

FIG.5C

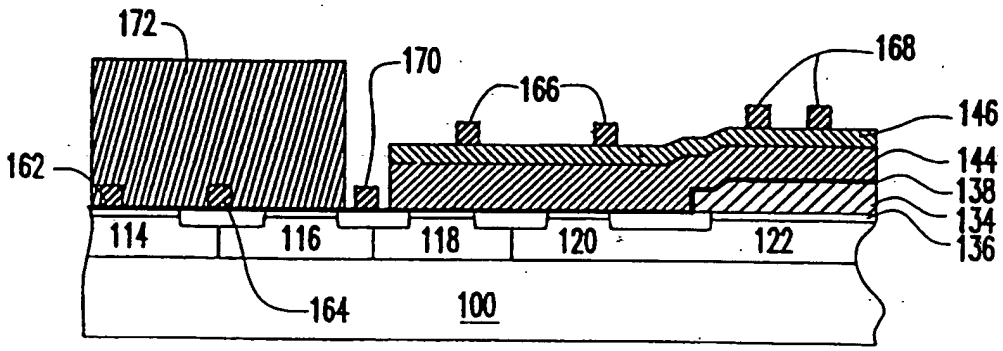

FIG.6A

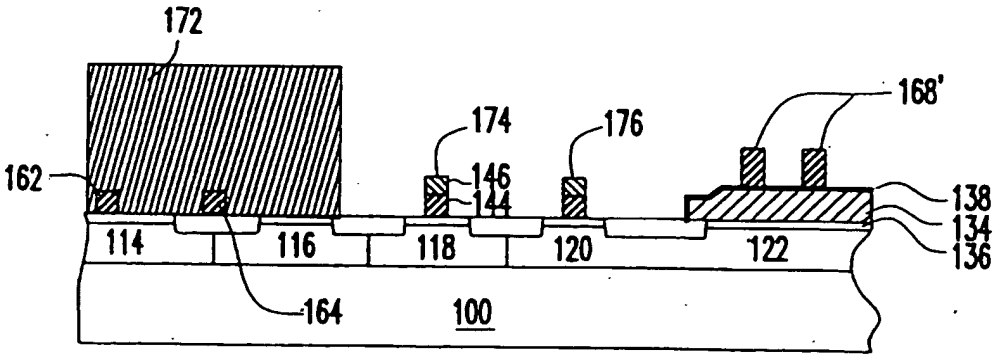

FIG.6B

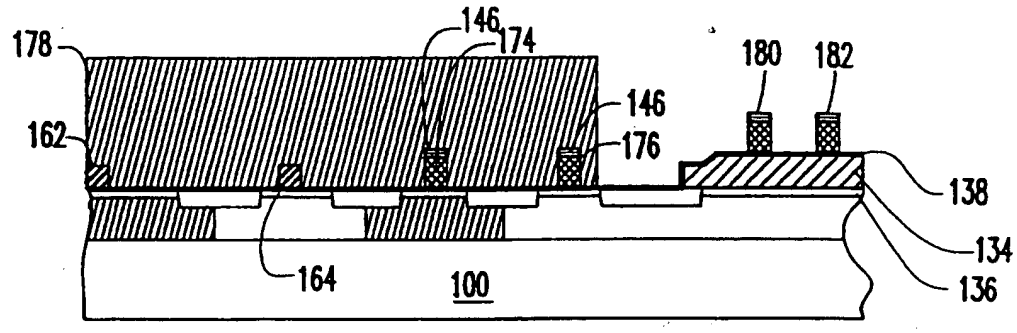

FIG.7A

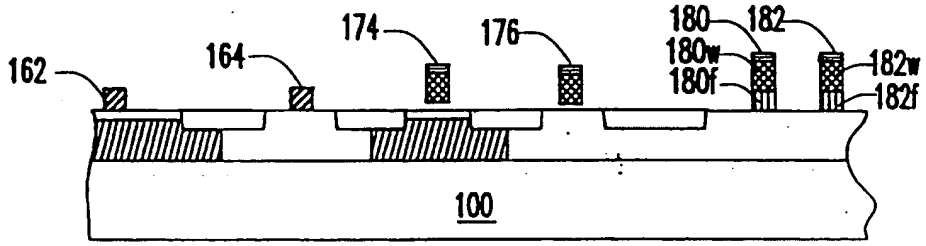

FIG.7B

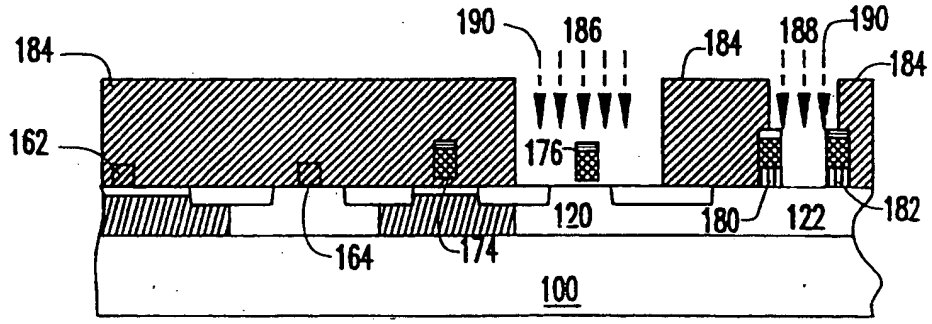

FIG.8A

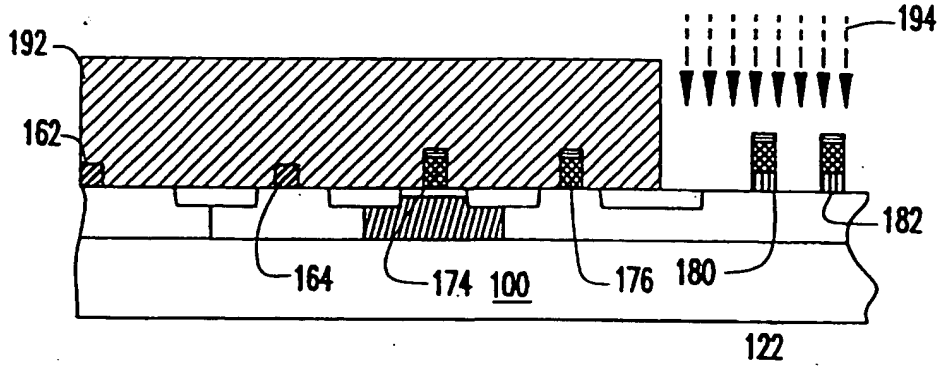

FIG.8B

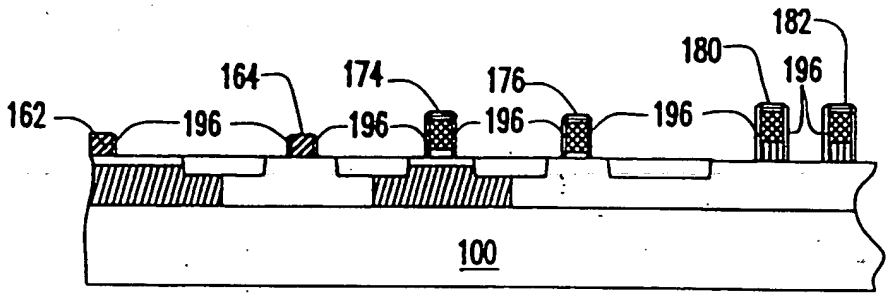

FIG.8C

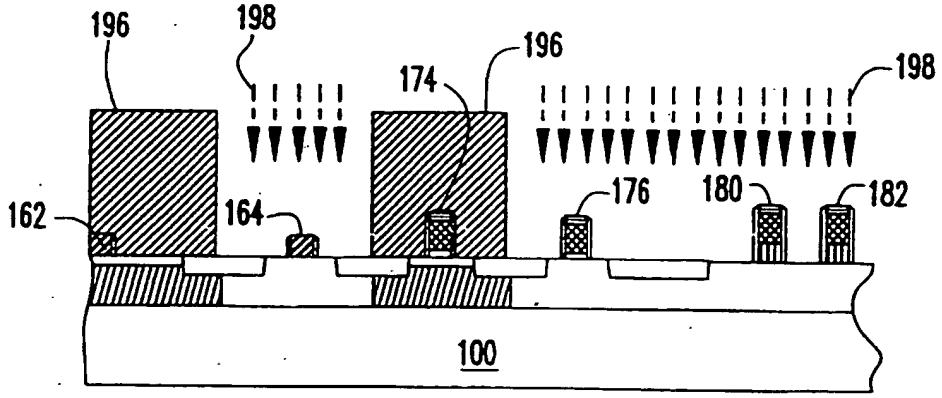

FIG.8D

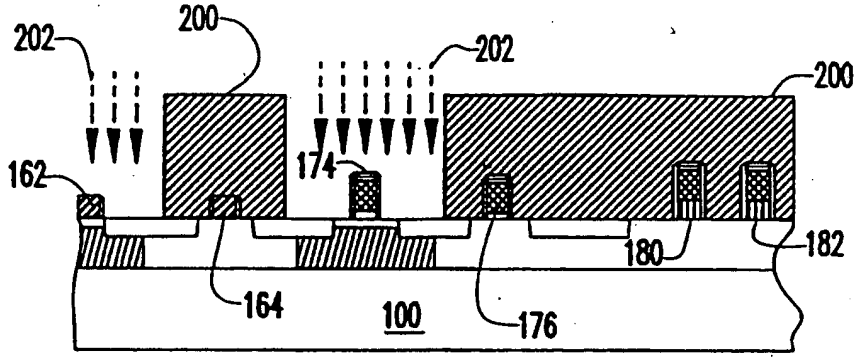

FIG.8E

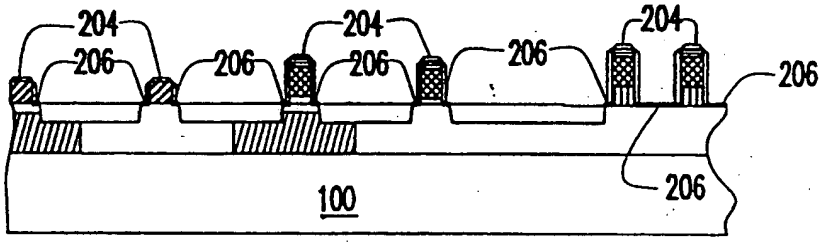

FIG.9

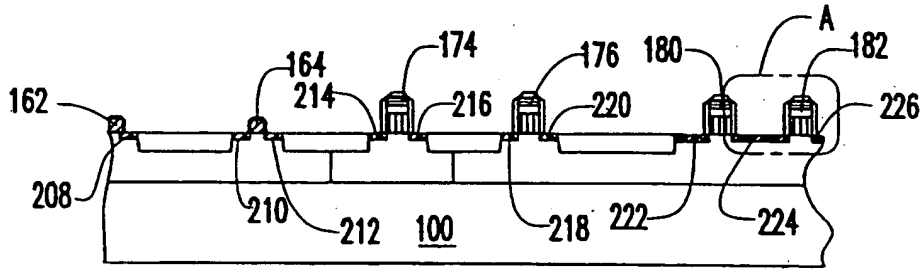

FIG.10

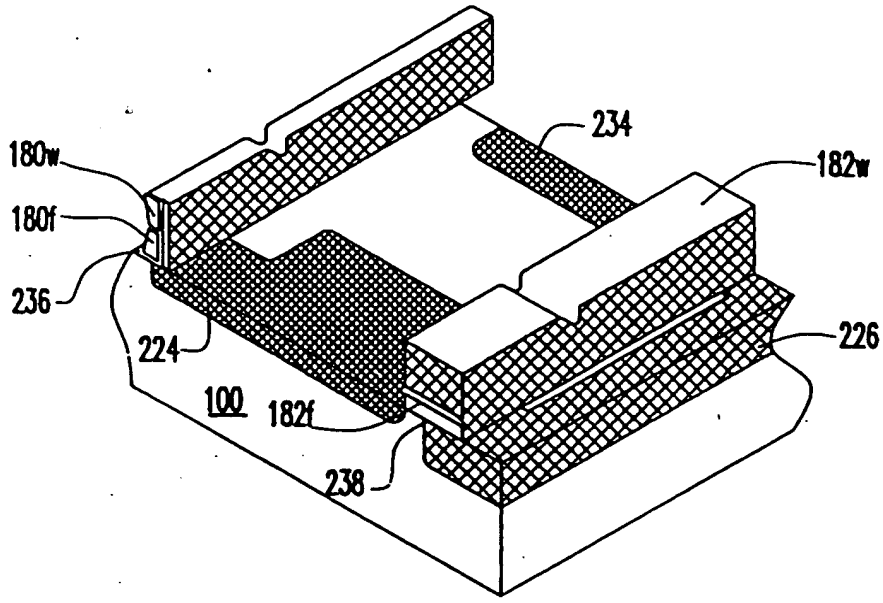

FIG.11A

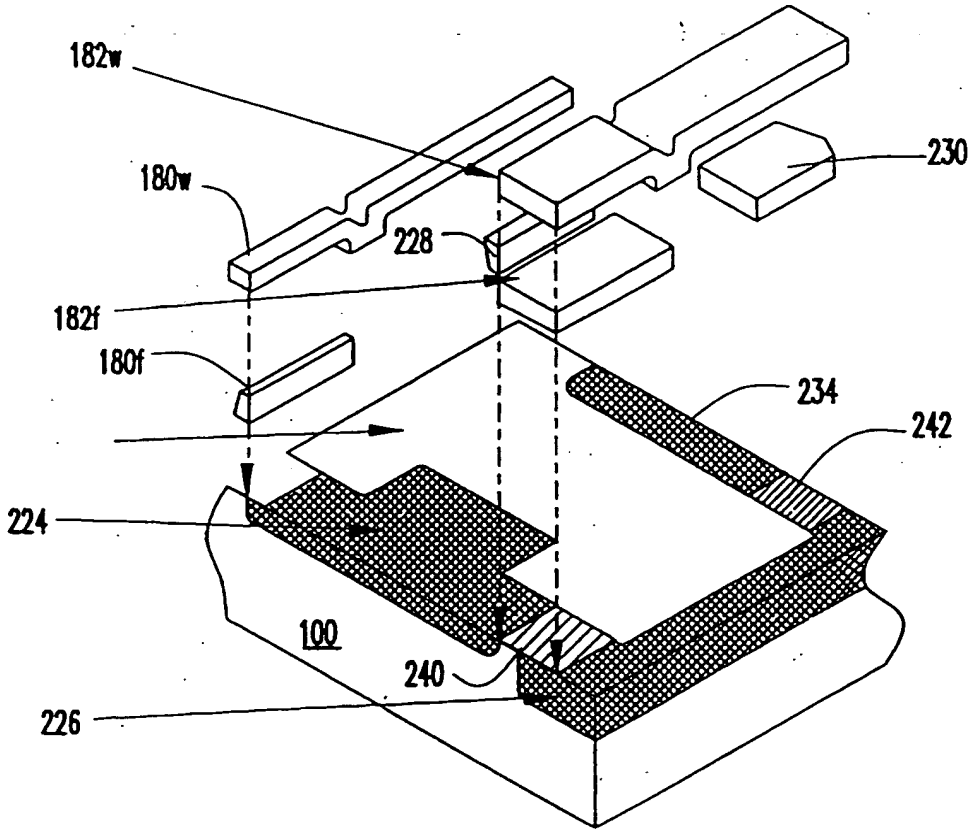

FIG.11B

TRIPLE POLYSILICON EMBEDDED VNRAM CELL

Field of the Invention

The present invention generally relates to non-volatile memory cells and more particularly to a three-dimensional, direct-write non-volatile random access memory (NVRAM) cell having a high integration density and fabrication methods thereof.

Background of the Invention

Non-volatile floating gate memory cells, such as in a non-volatile random access memory (NVRAM) arrays are well known in the industry. In NVRAM cells, the cell's conductive state is determined by the charge state of the cell's floating gate. The floating gate is an electrically isolated gate of a field effect transistor (FET) stacked in a two device NAND-like structure. Charge is forced onto or removed from the floating gate through a thin insulator layer that, normally (during a read operation), isolates the gate electrically from other adjoining conductive layers. Typically, a negatively charged floating gate is representative of a binary one state, while an uncharged floating gate is representative of a binary zero state. The other device in the NAND-like structure provides cell read and write selection.

For writing cells, a control gate (or program gate) is capacitively coupled to the floating gates in a portion of an array. A program voltage that is much higher than normal operating voltages, is placed on a control gate to bias the cell's floating gate sufficiently to change the charge on the cell's floating gate, i.e., to write selected cells.

However, typical program voltages, which range from 8-20 volts, are sufficiently high to destroy single gate FETs. Consequently, NVRAM chips require inclusion of special high voltage devices capable of handling these higher voltages without damage. Typical high voltage FETs have thicker gate oxides that are capable of withstanding the higher electric fields developed FETS by the presence of the programming voltage.

Typically, areas of the particular chip die were defined, lithographically. Unfortunately, exposing the thicker dielectric in these high voltage device areas to lithographic processing degraded the dielectric, causing failures, which degraded chip yield and, left residual contaminants that made these prior art devices less reliable.

Thus, there is a need for a semiconductor process for non-volatile memory wherein these gate oxide FETs may be included without degrading chip yield or reliability.

Disclosure of the Invention

The present invention is a logic chip including a non-volatile random access memory (NVRAM) array and method of fabrication thereof. The chip includes devices with gates on one or more of three polysilicon layers. Chip logic uses normal FETs and array support includes high voltage FETs. Both logic and support are CMOS. The gates of normal FETs in the chip logic are fashioned from the third or uppermost polysilicon layer. The third polysilicon layer also is used as a mask for high voltage FETs and array word lines, both of which use the second polysilicon layer for gates. The first polysilicon layer is used solely for cell floating gates.

Brief Description of the Drawings

The invention will now be described, by way of example only, with reference to the accompanying drawings, in which:

Figure 1 is a flow diagram of the preferred embodiment triple polysilicon method of forming a preferred embodiment integrated circuit including logic with embedded EEPROM cells;

Figures 2A-D show the semiconductor wafer preparation step;

Figure 3 show the step of forming a floating gate layer in cell areas;

Figures 4A-B show the step of forming a polysilicon high voltage gate layer;

Figures 5A-C show the step of defining logic device gates;

Figures 6A-B show the step of defining HiV gates and word lines;

Figures 7A-B show the step of defining individual cell floating gates;

Figures 8A-B show the step of implanting device source/drain diffusions;

Figure 9 shows the step of forming nitride on the device structure of Figure 8E;

Figure 10 shows the wafer after annealing to diffuse implanted source/drain dopant;

Figure 11A is an expanded plan view of EEPROM cell area A in Figure 10; and

Figure 11B is an exploded view of the EEPROM cells in area of Figure 11A

Detailed Description of the Invention

Referring now to the drawings, and more particularly to Figure 1, which is a flow diagram of the preferred method of forming a triple polysilicon integrated circuit including logic with embedded EEPROM cells. High voltage (HiV) devices are included to interface between the chip logic and EEPROM cells. The HiV FETs are capable of withstanding the higher than normal voltage operating conditions experienced during an erase or write operation.

First, in step 50, as shown in cross-section in Figures 2A-D a semiconductor wafer 100, preferably silicon, is prepared. In Figure 2A pad oxide 102 and pad nitride 104 are formed on the wafer 100. Preferably, the pad oxide layer 102 is 15nm thick and the pad nitride layer 104 is 172nm thick. Shallow isolation trenches 106, 108, 110 and 112 are defined, preferably lithographically. Then, trenches 106,108, 110 and 112 are etched through pad oxide 102, pad nitride 104 to a depth of about 500nm into the silicon wafer 100.

The preferred embodiment manufacturing process is a complementary insulated gate field effect transistor (FET) process commonly referred to as CMOS and includes both normal FETs and higher voltage FETs and floating gate cell devices. Thus, both normal FETs and higher voltage FETs, referred to herein as NFETs & PFETs in areas 114, 116, HiV NFETs & HiV PFETs in areas 118 and 120, respectively. Floating gate cell devices in areas 122 are referred to herein as EEPROM cell. The cross-section of the Figures is intended to illustrate formation of all five device variations.

Thus, having defined device areas 114, 116, 118, 120 and 122, the shallow trenches 206,108, 110 and 112 are filled with oxide, preferably

TEOS, and the filled structure is annealed at 1000°C for TEOS densification. Then, in Figure 2B the pad nitride layer 104 is stripped, preferably using a hot phosphoric acid wet etch and the surface 124 is planarized.

In Figure 2C, high voltage p-wells, for HiV NFETs 118 and EEPROM cells 122 are defined. A mask 126 protects NFET areas 114 as well as PFET areas 116 and HiV PFET areas 120. Using a two-step implant as represented by arrows 128, the unmasked surface areas of silicon wafer 100 are implanted to a level sufficient for high voltage threshold tailoring. First, boron is implanted 128 at 195KeV to a dopant level of $2.0x10^{12}$ cm^{-2}, followed by BF_2 at 75KeV to a dopant level of $8.0x10^{12}$ cm^{-2}. After this two-step implant, the mask 126 is removed using a dry strip and the wafer is cleaned using a S/N/O clean (sulfuric nitric ozone clean) to re-expose the surface 124.

Next, in Figure 2D, high voltage FET n-wells are formed for HiV PFETs 118. Again the surface 124 is masked 130 to protect normal PFET areas 116, normal NFET areas 114, HiV NFET areas 120 and EEPROM cells 122, while leaving HiV PFET areas 118 exposed. Like the high voltage p-wells, the high voltage n-wells are doped using a two-step doping as represented by arrows 132. First, arsenic is implanted at 1000KeV to a dopant level of $4.0x10^{13}$ cm^{-2}, followed by antimony at 140KeV to a dopant level of $2.0x10^{12}$ cm^{-2}. The resist 130 is stripped away using a dry strip and remaining pad oxide 102 is stripped from the surface 124. Thus, wafer preparation step 50 (of Figure 1) is complete.

Next, in step 52 (of Figure 1), as represented in Figure 3, a floating gate layer 134 is formed in cell areas. First, a 9.0nm tunnel oxide layer 136 is grown on the surface 124. Then, a 120.0nm amorphous polysilicon floating gate layer 134 is grown on the tunnel oxide 136. The floating gate layer 134 is implanted with a suitable dopant and an oxide-nitride-oxide (ONO) layer 138 is formed on the polysilicon floating gate layer 134. Preferably, the ONO layer 138 is formed by forming a 9.0nm dry oxide layer on the amorphous polysilicon floating gate layer 134, followed by deposition of an 8.5nm layer of nitride and a subsequent 1.5-2.0nm oxide layer. A mask pattern 140 is formed on the ONO layer 138 and the floating gate layer 134 is patterned by etching away exposed ONO and amorphous polysilicon. Remaining tunnel oxide on surface 124 is stripped away to re-expose the silicon surface 124 in device areas 114, 116, 118 and 120.

Next, in step 54 (of Figure 1), as illustrated in Figures 4A-E, a high voltage device gate oxide layer 142 in Figure 4A is formed on the bare surface 124. Then, a high voltage gate layer 144 of polysilicon is formed on the high voltage gate oxide layer. Preferably, the high voltage gate oxide layer is 23.5nm thick and the polysilicon gate layer 144 is 200.0nm thick. A thin, 4.0nm, oxide layer (not shown) is formed on the polysilicon high voltage gate layer 144. A nitride layer 146, preferably 120.0nm thick, is deposited on the thin oxide layer.

In Figure 4B, a mask 148 is formed on nitride layer 146 over HiV PFET areas 118, HiV PFET areas 120 and EEPROM areas 122. Then, portions of polysilicon high voltage gate layer 144, thin oxide layer and nitride layer 146 are selectively removed from PFET areas 114 and NFET areas 116. Once the resist 148 is removed in Figure 4C, the high voltage gate oxide layer is stripped away from the surface 124 in PFET areas 114 and NFET areas 116. This is followed by growing a temporary protective oxide layer (not shown), preferably 10.0nm thick, in PFET areas 114 and NFET areas 116.

Next, normal voltage FET n-wells and p-wells are defined. So, in Figure 4D, an n-well mask 150 is formed on the structure of Figure 4C and the n-wells are implanted, as represented by arrows 152. The n-well mask 150 is stripped away and a p-well mask, 154 in Figure 4B, is formed. The p-wells are implanted, as represented by arrows 156. Then, the p-well mask 154 is stripped away. The exposed surface is cleaned to remove the oxide layer and a gate oxide layer is formed. Preferably, the gate oxide is a 7.0nm thick layer grown in N_2O.

Then, in step 56 (of Figure 1) as represented in Figures 5A-C, logic device or normal FET gates are defined in areas 114, 116. In Figure 5A, a gate layer 158 of polysilicon is formed conformally. Preferably, gate layer 158 is 200.0nm thick and formed on the gate oxide layer. In Figure 5B, a mask pattern 160 is formed on the conformal polysilicon gate layer 158 to define the gates of all of the devices 114, 116, 118, 120 and 122. Preferably, the gate mask pattern 160 is formed using a well known TEOS hard mask technique. The conformal polysilicon gate layer 158 is selectively removed so that, in Figure 5C, PFET gates 162 and NFET gates 164 have been defined from the polysilicon gate layer 158. Additionally, a high voltage gate hard mask 166 and EEPROM gate hard mask 168 pattern is formed from the patterned polysilicon gate layer 158. Sidewall artifacts 170 remain along vertical edges.

Next, in step 58 (of Figure 1) as represented in Figures 6A-B, HiV gates and word lines are defined. In Figure 6A, PFET gates 162 and NFET gates 164 are masked 172 and a dry etch is applied to etch away exposed nitride 146, nitride remaining under mask pattern 160. This nitride etch is followed by a polysilicon etch, which removes masking polysilicon pattern 166, 168 and sidewall artifact 170 as it selectively removes high voltage gate layers 144 leaving, in Figure 6B, HiV PFET gates 174 and HiV NFET gates 176 in and word line stacks 180 and 182 running the length of the EEPROM array, i.e., out of the page. As seen, HiV PFET gates 174 and HiV NFET gates 176 and EEPROM gates 168' are comprised of portions of high voltage gate layers 144, 146. At this point, the sidewall artifacts 170 have also been removed. Etching ends at the ONO layer 138 on floating gate layer 134.

Then, in step 60 (of Figure 1), as represented in Figures 7A-B, individual cell floating gates are defined. Thus, Figure 7A illustrates the final floating gate definition step, wherein defined PFET gates 162, NFET gates 164, HiV PFET gates 174 and HiV NFET gates 176 masked 178. Exposed portions of ONO layer 138 are etched to re-expose unmasked portions of floating gate layer 134, which is subsequently selectively etched leaving word line stacks 180, 182 defining EEPROM cells in Figure 7B. Each EEPROM gate cell includes a floating gate 180f or 182f and a word line 180w or 182w. After defining PFET gates 162, NFET gates 164, HiV PFET gates 174, HiV NFET gates 176, word lines 180w, 182w, and floating gates 180f and 182f, source and drains diffusions may be implemented.

Then in step 62 (of Figure 1), as represented in Figures 8A-E device source/drain diffusions are implanted. In Figure 8A, a diffusion mask 184 is formed on the structure of Figure 7B to define areas for high voltage diffusion implant. Windows 186 and 188 are opened through the mask 184, leaving HiV NFET areas 120 exposed and windows 188 are opened leaving bit line contact areas exposed in EEPROM areas 122. Exposed areas are implanted (through the windows 186, 188) with phosphorous, as represented by arrows 190, to lightly dope both HiV NFET diffusions in areas 120 and EEPROM cell drain diffusions in bit line contacts in EEPROM areas 122. Then, the mask 184 is stripped away. Layer 146 has been stripped from word lines 180, 182 and HiV gates 174 176 by a hot phosphoric acid wet etch. In Figure 8B, mask 192 is formed, leaving only the EEPROM areas 122 exposed. Then, EEPROM cell source/drain diffusions are implanted with Arsenic in EEPROM areas 122.

Having implanted the EEPROM cells and HiV NFETs, in Figure 8C, nitride sidewalls 195 are formed on each of the gates 162, 164, 174 and 176 and word line stacks 180 and 182. Preferably, the nitride sidewalls 195 are formed by depositing a conformal layer of nitride, followed by a directional etch, e.g., a reactive ion etch (RIE); to remove nitride from horizontal surfaces.

Next, in Figure 8D, a mask 196 masks PFETs 114 and HiV PFETs 118 and the NFET devices are completed with a final n-type implant, as represented by arrows 198. During the implant NFET 198 n-type source/drain diffusions are defined simultaneously with doping NFET gates 164 and HiV NFET gates 176. Mask 196 is stripped away and in Figure 8E, mask 200, which is essentially a negative of mask 196, masks n-type regions, while PFET areas 114 and HiV PFET areas 118 are implanted with germanium and boron as represented by arrows 202, to define p-type source drain diffusions and dope gates 162, 174.

Next, in step 64 (of Figure 1) as represented in Figures 9 and 10, silicide is formed on the device structure. First, the mask 200 is stripped off of the wafer, preferably using a dry strip and, the wafer is cleaned. The wafer is annealed, preferably using a rapid thermal anneal, to activate dopants and repair any surface damage from dopant implants. A titanium layer is deposited, preferably using a sputter deposition technique. The titanium layer is annealed in nitrogen at to form Titanium Silicide on exposed regions. Then, unreacted Titanium is stripped from away, followed by a silicide transformation anneal, which leaves gates 162, 164, 174 and 176 and word line stacks 180 and 182 capped with $TiSi_2$ 204. Source/drain areas are also silicided. From this point, processing would continue with conventional back end of the line processing as is well known in the art.

Figure 11A is an expanded plan view of EEPROM cell area A in Figure 10. Figure 11B is an exploded view of the EEPROM cells of Figure 11A. Portions of four cells are shown in Figures 11A-B as represented by floating gate 182f and floating gate portions 180f, 228 and 230. Word line 180 is capacitively coupled to floating gates 180f and 228, while word line 182 is capacitively coupled to floating gates 182f and 230. Each bit line diffusion 224, 232 is shared by four cells; only two of which are shown for each bit line diffusion 224, 234 of Figures 11A-B. A source line 222, 226 runs parallel to and, provides the source voltage for cells on one Word line 180w, 182w, respectively. Tunnel oxide 236, 238 between the floating gates 180f, 182f, 228, 230 and the surface 124 facilitates cell programming.

During erase, previously stored (written) electrons on the floating gate 180f, 182f, 228, 230 tunnel to source line 222, 226 through the tunnel oxide 236, 238. During a write, electrons are injected from the channel 240, 242 to the floating gate 180f, 182f, 228, 230.

During a read operation, the FET of the floating gate will either go to the "ON" state or stay in the "OFF" state when the wordline is selected, depending on the electron charge stored in the floating gate. Thus, cells such as in Figures 11A-B may be programmed, read, erased and reprogrammed by applying voltages to cell terminals as set forth in the table below.

	READ	WRITE	ERASE
Bit line	1v	"0" = 5V "1" = 0V	floating
Word line	3V	10v	0v
Source line	0v	0v	10v

Having thus formed the preferred embodiment integrated circuit chip, including logic and an embedded non-volatile array, e.g., a microprocessor with embedded flash memory, the triple polysilicon process of the preferred embodiment provides an integrated circuit logic chip with an embedded EPROM array without suffering the dilatory effects of prior art semiconductor processes.

CLAIMS

1. An integrated circuit logic (IC) chip comprising:

a non-volatile random access memory (NVRAM) array of one or more of NVRAM cells, each of said cells including:

a floating gate between a bit line and a source line, said floating gate being on a first conduction layer, and a Word line device on a second conduction layer;

cell selection circuits, said cell selection circuits including a plurality of first FETs having gates on said second conduction layer; and a plurality of logic gates including a plurality of second FETs having gates on a third conduction layer, said cell selection circuits selecting cells in said array responsive to said plurality of logic gates, said plurality of logic gates receiving selected data from said array.

2. An IC chip as claimed in claim 1, wherein said first FETs have a thicker gate dielectric than said second FETs.

3. An IC chip as claimed in claim 2, wherein said first FETs includes one or more FETs of a first conduction type and one or more FETs of a second conduction type.

4. An IC chip as claimed in claim 3, wherein said second FETs includes one or more FETs of a said conduction type and one or more FETs of said second conduction type.

5. An IC chip as claimed in claim 4, wherein each said floating gate includes a tunnel oxide on a floating gate channel between said bit line and said source line, said tunnel oxide being thicker than gate dielectric of said second FETs.

6. An IC chip as claimed in claim 5, wherein said chip is a silicon IC chip, said gate dielectric is SiO_2, said tunnel oxide is 9.0nm, said first FETs have a 22.5nm thick gate oxide and said second FETs have a 7.0nm thick gate oxide.

7. A method of forming an integrated circuit chip, said integrated circuit chip including a plurality of logic circuits having an embedded non-volatile random access memory (NVRAM) array, said method comprising the steps of

a) defining device areas on a semiconductor wafer, said device areas including array areas, first device type areas and second device type areas;

b) selectively forming a floating gate layer on said semiconductor wafer in said array areas;

c) selectively forming a first gate layer on said semiconductor wafer in said first device areas and on said floating gate layer;

d) forming a second gate layer on said semiconductor wafer in said second device type areas an on said first gate layer;

e) defining device gates in each of said areas; and

f) forming source and drain diffusions at said defined device gates.

8. A method as claimed in claim 7, wherein the step (a) of defining device areas comprising:

1) forming isolation trenches in a surface of a semiconductor wafer; and

2) forming isolation wells in said array areas and said first device type areas.

9. A method as claimed in claim 8, wherein the semiconductor wafer is a silicon wafer and the step (b) of selectively forming the floating gate layer comprises:

1) forming a tunnel oxide on said surface;

2) forming a polysilicon layer on said tunnel oxide; and3) etching said polysilicon layer, said polysilicon layer being removed from said first device type areas and said second device type areas.

10. A method as claimed in claim 9, wherein the step (b) of selectively forming the floating gate layer further comprises, before the step (3) of etching the polysilicon layer, the step of:

2A) forming an oxide-nitride-oxide (ONO) layer on said polysilicon layer.

11. A method as claimed in claim 9, wherein the step (c) of selectively forming the first gate layer comprises the steps of:

1) forming a first gate oxide layer on said silicon surface;

2) forming a polysilicon layer on said first gate oxide layer; and

3) etching said polysilicon layer, said polysilicon layer being removed from said second device type areas.

12. A method as claimed in claim 11 wherein the step (c) of selectively forming the first gate layer further comprises, before the step (3) of etching the polysilicon layer, the step of:

2A) forming an oxide and nitride layer on said polysilicon layer.

13. The method as claimed in claim 11, wherein the step (d) of forming the second gate layer comprises the steps of:

1) forming isolation wells in said second device type areas;

2) forming a second gate oxide layer on said silicon surface; and

3) forming a polysilicon layer on said second gate oxide layer.

14. A method as claimed in claim 13, wherein the step (e) of defining device gates layer comprises the steps of:

1) patterning said second gate layer, said patterned second gate layer defining gates in said second device type areas and a mask pattern in said first device type areas and said array areas;

2) defining first gates in said first device type areas and word lines in said array areas; and

3) defining floating gates in said array areas.

15. A method as claimed in claim 14, wherein the first gate layer includes a dielectric layer on said polysilicon layer and, the step (2) of defining first gates and word lines comprises the steps of:

A) forming a protective layer over said defined second gates;

B) removing said dielectric layer, said polysilicon layer in said first gate layer being exposed between shapes of said mask pattern; and

C) etching said exposed polysilicon layer.

16. A method as claimed in claim 15, wherein the floating gate layer includes a dielectric layer on said polysilicon layer and, the step (3) of defining the floating gates comprises the steps of:

A) forming a protective layer over said defined first gates and second gates;

B) removing said dielectric layer, said polysilicon layer in said floating gate layer being exposed between said word lines; and

C) etching said exposed polysilicon layer.

17. A method as claimed in claim 16, wherein the step (f) of forming source and drain diffusions comprises the steps of:

1) implanting dopant into source and drain areas;

2) diffusing said implanted dopant;

3) forming a nitride layer on said defined gates and said implanted source and drain areas;

4) implanting and diffusing said standard logic FETs; and

5) forming a silicide on said defined gate and said implanted source and drain area.

18. A method as claimed in claim 17, wherein said tunnel oxide is grown to a thickness of 9.0nm, said first gate oxide is grown to a thickness of 23.5nm and said second gate oxide is grown to a thickness of 7.0nm.

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Claims searched: All **Date of search:** 27 April 2000

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Search Report under Section 17

Databases searched:

UK Patent Office collections, including GB, EP, WO & US patent specifications, in:

UK Cl (Ed.R): H1K (KDEG, KGAGF)

Int Cl (Ed.7): H01L 21/8239, 21/8246, 21/8247, 27/112, 27/115, 29/788

Other: Online: EPODOC, JAPIO, WPI

Documents considered to be relevant:

Category	Identity of document and relevant passage		Relevant to claims
A	EP 0892430 A1	(ST MICROELECTRONICS) See whole document	
A	EP 0379449 A1	(SGS-THOMSON) See abstract	
A	US 5756385	(YUAN) See whole document	
A	US 5587332	(CHANG) See column 4 lines 13 to 60 in particular	

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